Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) A data transfer control system connected to a bus for controlling a data transfer to a device on the bus, comprising:

data storing means for storing data;

transferred-word number storing means for storing the number of words of data which are to be transferred;

transfer interval storing means for storing an interval between destination addresses, the destination addresses, to which a plurality of one-word data included in the data are to be transferred, being equally-separated with the interval; and

bus cycle controlling means for controlling the data transfer such that, during a burst transfer, in a single bus cycle, during the single bus cycle, the bus is driven continuously and a write control line of the bus is placed in a write-enabled state for a one-word data transfer period and is placed in a write-disabled state for an (N-1) words data transfer period and the operation is repeated for [[M(1<M)]] M(2<M) times periodically, the M being the number of words of data which are to be transferred and stored in the transferred-word number storing means,

wherein N is the number stored in the transfer interval storing means, and that data including a number of words which is equal to the number stored in the transferred-word number storing means is transferred while the write control line is in the write-enabled state.

3. (Original) The data transfer control system of claim 2, further comprising:

cycle start address storing means for storing a start address of a bus cycle;

resumption address calculating means for calculating a destination address of second data when being informed by the device about interruption of the data transfer during the time when the data transfer is performed in the write-disabled state; and

interrupted-cycle resuming means for transferring the address calculated by the resumption address calculating means to the cycle start address storing means to start a new bus cycle from the address stored in the cycle start address storing means when being informed by the device about interruption of the data transfer during the time when the data transfer is performed in the write-disabled state.

4. (Original) The data transfer control system of claim 2, further comprising:

response speed storing means for storing a device response speed of a target device;

transfer speed comparing means for comparing the data transfer rate in a burst transfer mode with the data transfer rate in a data transfer mode where transfer of one-word data to a destination address is repeated, based on the values of the transfer interval storing means and the response speed storing means; and

transfer mode selecting means for selecting the burst transfer mode if the data transfer rate is faster in the burst transfer mode than in the data transfer mode where transfer of one-word data to a destination address is repeated and, if otherwise, selecting the data transfer mode where one-word data transfer bus cycle for a destination address is repeated.

5. (Original) The data transfer control system of claim 3, further comprising:

response speed storing means for storing a device response speed of a target device;

transfer speed comparing means for comparing the data transfer rate in a burst transfer mode with the data transfer rate in a data transfer mode where transfer of one-word data to a destination address is repeated, based on the values of the transfer interval storing means and the response speed storing means; and

transfer mode selecting means for selecting the burst transfer mode if the data transfer rate is faster in the burst transfer mode than in the data transfer mode where transfer of one-word data to a destination address is repeated and, if otherwise, selecting the data transfer mode where one-word data transfer bus cycle for a destination address is repeated.

6. (Original) The data transfer control system of claim 2, wherein the bus cycle controlling means drives next one-word data to be transferred onto a data line when the write control line is in the write-disabled state.

7. (Original) The data transfer control system of claim 3, wherein the bus cycle controlling means drives next one-word data to be transferred onto a data line when the write control line is in the write-disabled state.

8. (Original) The data transfer control system of claim 4, wherein the bus cycle controlling means drives next one-word data to be transferred onto a data line when the write control line is in the write-disabled state.

9. (Cancelled)

10. (Cancelled)

11. (Withdrawn) A data transfer control system connected to a bus for controlling a data transfer to a device on the bus, comprising:

data storing means for storing data;

transferred-word number storing means for storing the number of words of data which are to be transferred;

non-transfer interval storing means for storing an interval between addresses to which the data is not to be transferred;

bus cycle controlling means for controlling the data transfer such that, during a burst transfer, in a single bus cycle, during the single bus cycle, the bus is driven continuously and a write control line of the bus is placed in a write-disabled state for a one-word data transfer period and is placed in a write-enabled state for an (N-1) words data transfer period periodically, wherein N is the number stored in the non-transfer interval storing means, and that data including a number of words which is equal to the number stored in the transferred-word number storing means is transferred while the write control line is in the write-enabled state.

12. (Currently Amended) A data transfer control method for controlling a data transfer to a device on a bus, comprising:

a data storing step of storing data;

a transferred-word number storing step of storing the number of words of data which are to be transferred;

a transfer interval storing step of storing an interval between data destination addresses, the destination addresses, to which a plurality of one-word data included in the data are to be transferred, being equally-separated with the interval; and

a bus cycle controlling step of controlling the data transfer such that, during a burst transfer, in a single bus cycle, during the single bus cycle, the bus is driven continuously and a write control line of the bus is placed in a write-enabled state for a one-word data transfer period and is placed in a write-disabled state for an (N-1) words data transfer period and the operation is repeated for [[M(1<M)]] M(2≤M) times periodically, the M being the number of words of data which are to be transferred and stored in the transferred-word number storing step,

wherein N is the number stored in the transfer interval storing step, and that data including a number of words which is equal to the number stored at the transferred-word number storing step is transferred while the write control line is in the write-enabled state.